| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/823,293 | WANG ET AL. | |
| | Examiner | Art Unit | |
| | Habte Mered | 2616 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *communication filed on 12/04/2006*.

2. ☒ The allowed claim(s) is/are *1-17*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Attachment A*.

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

## EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Arthur T. C. Au on 6/19/2007.

3. The claims have been amended as shown in Attachment A.

### *Allowable Subject Matter*

4. **Claims 1-17** are allowed.

5. The following is an examiner's statement of reasons for allowance:

6. **Claims 1-6** are allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest a method of buffering or reading path overhead bytes by identifying a plurality of path overhead bytes as they are received and selecting a subset of path overhead bytes from the plurality of path overhead bytes and determining a path overhead number (P#) for each byte of the selected subset of path overhead bytes and determining a signal number (S#) for each byte of the selected subset of path overhead bytes and storing the selected path overhead bytes, signal numbers (S#), and path overhead numbers (P#) into three different sections of a RAM FIFO buffer. It is noted that the closest prior art, Hamlin et al (R. W. Hamlin, Jr., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), discloses a SONET/SDH Overhead Terminator to

process TOH and POH bytes independently but buffers all the incoming and the outgoing overhead bytes as well as the performance monitor counters in an on-chip RAM without correlating the path overhead bytes to a specific SONET STS frame.

7. **Claims 7-11** are allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest a method of buffering or reading path overhead bytes by identifying a plurality of path overhead bytes as they are received and selecting a subset of path overhead bytes from the plurality of path overhead bytes and determining a path overhead number (P#) for each byte of the selected subset of path overhead bytes and determining a signal number (S#) for each byte of the selected subset of path overhead bytes and storing a first subset of the selected path overhead bytes, signal numbers (S#), and path overhead numbers (P#) into three different sections of a first RAM FIFO buffer and storing a second subset of the selected path overhead bytes, signal numbers (S#), and path overhead numbers (P#) into three different sections of a second RAM FIFO buffer. It is noted that the closest prior art, Hamlin et al (R. W. Hamlin, Jr., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), discloses a SONET/SDH Overhead Terminator to process TOH and POH bytes independently but buffers all the incoming and the outgoing overhead bytes as well as the performance monitor counters in an on-chip RAM without correlating the path overhead bytes to a specific SONET STS frame.

8. **Claims 12-14** are allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest an

apparatus comprising a RAM FIFO buffer having a plurality of entries wherein each entry comprises a first section for storing a path overhead byte selected from a plurality of path overhead bytes for a synchronous payload envelope of a SONET frame, a second section for storing a signal number (S#) and a third section for storing a path overhead number (P#) wherein the path overhead number (P#) correlates to the path overhead byte stored in the first section effectively showing which path overhead byte for the synchronous payload envelope for the SONET frame is stored. It is noted that the closest prior art, Hamlin et al (R. W. Hamlin, Jr., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), discloses a SONET/SDH Overhead Terminator to process TOH and POH bytes independently but buffers all the incoming and the outgoing overhead bytes as well as the performance monitor counters in an on-chip RAM without correlating the path overhead bytes to a specific SONET STS frame.

9. **Claims 15-17** are allowable over the prior art of record since the cited references, taken individually or in combination, fail to particularly teach or suggest an apparatus comprising a first RAM FIFO buffer and a second RAM FIFO buffer wherein the first RAM FIFO buffer has a plurality of entries wherein each entry comprises a first section for storing a first set of path overhead bytes derived from a group of one or more byes selected from a plurality of path overhead bytes for a synchronous payload envelope of a SONET frame, a second section for storing at least a portion of a signal number (S#) and a third section for storing a path overhead number (P#) wherein the path overhead number (P#) correlates to the first set of path overhead bytes stored in

the first section effectively showing which path overhead byte for the synchronous payload envelope for the SONET frame is stored; and the second RAM FIFO buffer has a plurality of entries wherein each entry comprises a first section for storing a second set of path overhead bytes derived from a group of one or more byes selected from a plurality of path overhead bytes for the synchronous payload envelope of a SONET frame, a second section for storing at least a portion of a signal number (S#) and a third section for storing a path overhead number (P#) wherein the path overhead number (P#) correlates to the first set of path overhead bytes stored in the first section effectively showing which path overhead byte for the synchronous payload envelope for the SONET frame is stored and further the first set of path overhead bytes correspond to a first set of signal numbers and the second set of path overhead bytes correspond to a second set of signal numbers. It is noted that the closest prior art, Hamlin et al (R. W. Hamlin, Jr., "A SONET/SDH Overhead Terminator for STS-3, STS-3C, and STM-1", 1993, IEEE), discloses a SONET/SDH Overhead Terminator to process TOH and POH bytes independently but buffers all the incoming and the outgoing overhead bytes as well as the performance monitor counters in an on-chip RAM without correlating the path overhead bytes to a specific SONET STS frame.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H. To can be reached on 571 272 7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HM
06-20-2007

Attachment A

**IN THE CLAIMS:**

Applicants amended claims 12 and 15. No claims have been added or canceled. The listing of claims replaces all prior versions, and listings, of claims in the application.

**LISTING OF CLAIMS:**

1. (Previously Presented) In a digital optical network, a method of buffering and reading path overhead bytes, comprising:

identifying a plurality of path overhead bytes as they are received;

selecting a subset of path overhead bytes from said plurality of path overhead bytes;

determining a signal number (S#) for each byte of said subset of path overhead bytes;

determining a path overhead number (P#) for each byte of said subset of path overhead bytes based on which one of said path overhead bytes is selected;

storing path overhead bytes, signal numbers (S#), and path overhead numbers (P#) into a RAM FIFO buffer, wherein the RAM FIFO comprises a plurality of entries, each entry comprising a first section for storing a path overhead byte, a second section for storing a signal number (S#), and a third section for storing a path overhead number (P#); and

reading said entries from the RAM FIFO, wherein said entries are stored and read from the RAM FIFO in accordance with a first-in-first-out (FIFO) protocol.

2. (Original) The method of claim 1 further comprising:

incrementing a first counter each time one of said path overhead bytes is stored in one of said entries;

incrementing a second counter for each entry that is read;

determining when a difference in values between said first counter and said second counter reaches a specified value (N);

generating an interrupt signal when the difference reaches N;

transmitting the interrupt signal to a processor; and

initiating said step of reading when the interrupt signal is received by the processor.

3. (Original) The method of claim 1 further comprising:

incrementing a first counter each time one of said path overhead bytes is stored in one of said entries;

incrementing a second counter for each entry that is read;

periodically polling said first and second counters at specified time intervals to determine a difference in values between the first and second counters; and

initiating said step of reading when the difference reaches a specified value.

4. (Original) The method of claim 1 wherein said step of reading comprises burst mode reading of entries from said RAM FIFO.

5. (Original) The method of claim 1 wherein said step of reading comprises direct memory access (DMA) reading of entries from said RAM FIFO.

6. (Original) The method of claim 1 wherein said step of storing comprises storing only path overhead bytes meeting desired criteria, wherein said desired criteria includes any combination of said signal numbers (S#) and said path overhead numbers (P#).

7. (Previously Presented) In a digital optical network, a method of buffering and reading path overhead bytes, comprising:

identifying a plurality of path overhead bytes as they are received;

selecting one or more bytes of said plurality of path overhead bytes;

determining a signal number (S#) for each byte of said path overhead bytes selected;

determining a path overhead number (P#) for each byte of said path overhead bytes selected;

storing a first subset of said path overhead bytes, signal numbers (S#), and path overhead numbers (P#) in a first RAM FIFO buffer, wherein the first RAM FIFO includes a plurality of entries, each entry comprising a first section for storing a respective path overhead byte, a second section for storing at least a portion of a respective signal number (S#), and a third section for storing a respective path overhead number (P#), wherein said first subset of path overhead bytes have signal numbers corresponding to a first set of values;

storing a second subset of said path overhead bytes, signal numbers (S#), and path overhead numbers (P#) in a second RAM FIFO buffer, wherein the second RAM FIFO includes a plurality of entries, each entry comprising a first section for storing a respective path overhead byte, a second section for storing at least a portion of a respective signal number (S#), and a third

section for storing a respective path overhead number (P#), wherein said second subset of path overhead bytes have signal numbers corresponding to a second set of values; and

reading said entries from the first and second RAM FIFOs, wherein entries are stored and read from each respective first and second RAM FIFO in accordance with a first-in-first-out (FIFO) protocol.

8. (Original) The method of claim 7 wherein said step of reading comprises reading said first and second RAM FIFOs in parallel.

9. (Original) The method of claim 7 wherein said step of reading comprises burst mode reading said first and second RAM FIFOs in parallel.

10. (Original) The method of claim 7 wherein said step of reading comprises direct memory access (DMA) reading said first and second RAM FIFOs in parallel.

11. (Original) The method of claim 7 wherein said steps of storing comprise storing only path overhead bytes meeting desired criteria into said respective first and second RAM FIFOs, wherein said desired criteria includes any combination of said signal numbers (S#) and said path overhead numbers (P#).

12. (Currently Amended) An apparatus for buffering path overhead bytes, comprising:

a RAM FIFO buffer having a plurality of entries, each entry comprising a first section for storing a path overhead byte selected from a plurality of path overhead bytes for a synchronous payload envelope of a SONET frame, a second section for storing a signal number (S#) and a third section for storing a path overhead number (P#), ~~that correlates to which path overhead byte of said synchronous payload envelope is stored~~wherein the path overhead number (P#) correlates to the path overhead byte stored in the first section for the synchronous payload envelope of the SONET frame.

13. (Original) The apparatus of claim 12 wherein each entry of said plurality of entries comprises sixteen bits of storage capacity, said first section comprises eight bits of storage capacity, said second section comprises four bits of storage capacity, and said third section comprises four bits of storage capacity.

14. (Original) The apparatus of claim 12 further comprising:

a first counter that is incremented each time one of said path overhead bytes is stored in one of said entries; and

a second counter that is incremented for each of said entries that is read from said RAM FIFO.

15. (Currently Amended) An apparatus for buffering path overhead bytes, comprising:

a first RAM FIFO buffer having a first plurality of entries for storing a first set of path overhead bytes derived from a group of one or more bytes selected from

a plurality of path overhead bytes for a synchronous payload envelope of a SONET frame, wherein each of said first plurality of entries comprises a first section for storing a path overhead byte, a second section for storing at least a portion of a signal number (S#), and a third section for storing a path overhead number (P#) ~~that correlates to which path overhead byte of said synchronous payload envelope is stored~~, wherein the path overhead number (P#) correlates to the first set of path overhead bytes stored for the synchronous payload envelope of the SONET frame; and

a second RAM FIFO buffer having a second plurality of entries for storing a second set of path overhead bytes derived from one or more bytes of said plurality of path overhead bytes for said synchronous payload envelope, wherein each of said second plurality of entries comprises a first section for storing a path overhead byte, a second section for storing at least a portion of a signal number (S#), and a third section for storing a path overhead number (P#) that correlates to which path overhead byte of said synchronous payload envelope is stored, wherein said first set of path overhead bytes correspond to a first set of signal numbers and said second set of path overhead bytes correspond to a second set of signal numbers.

16. (Original) The apparatus of claim 15 wherein each entry of said first and second plurality of entries comprises sixteen bits of storage capacity, each of said first sections comprises eight bits of storage capacity, each of said second sections comprises four bits of storage capacity, and each of said third sections comprises four bits of storage capacity.

17. (Previously Presented) The apparatus of claim 15 further comprising:

a first counter that is incremented each time data an entry is stored in one of said first and second RAM FIFO; and

a second counter that is incremented for each entry that is read from said first and second RAM FIFOs.